Interface Barrier Technologies in Advanced Semiconductor Interconnect Metals and Their Reliability Impact: The Evolution from Cu to Co/Ru

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Abstract. In the sub-10 nm regime of interconnect, as the dimensions between the backends are becoming smaller, a coupled electrical, reliability, and manufacturability crisis is experienced with the traditional Cu/low-k dual-damascene platform, which is based on a Ta/TaN barrier, a liner stack and a Cu conductor. It is not only the resistivity size effect of Cu alone that functions as a bottleneck, but also the harsh loss of effective conducting cross-section to high-resistivity barrier/liner layers, the reinforcement of interface scattering, and the attendant increase in risks of electromigration, time-dependent dielectric breakdown and thermomechanical failure. This paper reviews the evolution of interface barrier technologies in advanced interconnects, examines the scaling limits of the conventional Cu/Ta (TaN) scheme, and analyzes representative routes including Co-W, Ru-Ta, atomically thin 2D materials, graphene encapsulation, Co-Ti single barrier/liner layers, Ru-Zn self-forming barriers, and Ru semi-damascene integration. The central argument is that the competition in advanced interconnects has shifted from simply identifying the metal with the lowest bulk resistivity to co-designing low-size-effect metals, ultrathin functional interfaces, and new integration architectures to minimize effective line resistance while maximizing reliability. Interface barriers are therefore no longer passive diffusion blockers; they are the functional layers that will decide whether post-Cu interconnect technologies can be industrialized.

Keywords: advanced interconnects, diffusion barriers, cobalt interconnects, ruthenium interconnects, electromigration, TDDB, semi-damascene.

1. Introduction

For more than two decades, the Cu/low-k dual-damascene platform has remained the industrial workhorse of backend interconnect integration. Its success was not due to the low bulk resistivity of Cu alone, but to a mature interface-engineering ecosystem in which Ta/TaN acts as the diffusion barrier, Ta, Co, or Ru-based liners provide adhesion and wetting, and seed plus electrofill processes deliver high-yield structures. Once the critical dimensions of interconnects moved into the 10 nm regime and below, however, interconnects ceased to be a secondary parasitic concern and became a first-order limiter of delay, energy consumption, and layout density. Gall showed that the resistivity of narrow Cu and Co conductors can rise to an order of magnitude above the bulk values because surface and grain-boundary scattering dominate transport in highly confined lines [1], while the broader materials review in MRS Bulletin emphasized that further scaling now depends on new materials and new interface treatments rather than on conventional metallization optimization alone [2].

The crisis of the Cu platform is fundamentally an interface crisis. The traditional barrier/liner stack remains chemically effective, but it becomes geometrically self-defeating at advanced nodes. If the Ta/TaN stack is thinned further, continuity and pinhole-free coverage degrade; if its thickness is preserved, the high-resistivity interface stack consumes an intolerably large fraction of the trench cross-section and increases diffuse scattering at the metal/interface boundary. Li et al. summarized this dilemma very clearly: direct electrochemical Cu deposition on Ta/TaN is unrealistic because of its high resistivity, so Cu seed deposition is unavoidable, but once the seed becomes non-uniform in sub-20 nm and especially sub-10 nm structures, void-free fill is immediately jeopardized [3].

Therefore, advanced interconnect scaling is no longer about whether Cu is intrinsically good enough; it is about whether the Cu-plus-interface system can remain viable under extreme confinement.

Recent literature has thus evolved along two intertwined trajectories. The first attempts to prolong the life of the Cu platform by replacing conventional Ta/TaN with thinner, more conductive, or more adhesion-friendly alternatives such as Co-W, Ru-Ta, atomically thin 2D materials, and graphene-enabled interface schemes [4-7]. The second path is more radical and drives the predominant conductor itself to Co and Ru and links the novel metals to single barrier/liner schemes, self-forming barriers, direct metal etch, and semi-damascene patterning [8-13]. The function of the interface barrier also has been redefined in both scenarios: no longer can it be used as a simple diffusion-blocking layer, but it must now be an ultrathin multi-purpose interface able to resistively isolate, bond, nucleate, be thermally stable, and reliable. This is the logic of this paper. It initially reexamines the physical principles underlying the interconnect scaling, followed by the lifetime-extension approaches in the Cu system and the paradigm shift posed by Co and Ru, and finally the effect of interface barrier layers to change the predominant electromigration, TDDB, and thermomechanical failure pathways.

2. Physical basis of interconnect scaling and the re-evaluation of interface barrier layers

2.1. Resistivity size effect and the role of electron mean free path

The bulk resistivity cannot be used to rank advanced interconnect materials anymore since transport in narrow wires is dominated by the boundaries. At larger values of the line width, thickness and grain size than the electron mean free path, the phonon and impurity scattering dominate resistivity. Surface and grain-boundary scattering effects become the bottlenecks in transport once these dimensions approach the mean free path. The balance between the specular reflection and the diffuse reflection at the interface controls surface scattering in the FuchsSondheimer description; the grain boundaries serve as internal reflectors in the MayadasShatzkes picture that degrade carrier momentum. Gall's reported typical mean free path values of about 39 nm for Cu, 19 nm for Co, and 6.7 nm for Ru immediately suggest that Cu would be far more responsive to interfacial roughness and microstructure disorder than Ru once the line width is reduced to of the order of 10 nm [1].

This is the cause of the first reason why the historical intuition of conduction of copper being the best loses predictive power on extreme confinement. With more complex interconnects, the most important thing is not the lowest bulk resistivity but the lowest effective line resistance when the volume penalty of the interface stack and the scattering penalty of the interfaces both have been taken into consideration. That is exactly what is stated in the review of interconnect materials in MRS Bulletin: the new generation of backend conductors needs to be considered along with the barrier/liner thickness, scattering suppression and manufacturability and not as an isolated bulk material [2]. The Cu/Co/Ru transition is thus enabled by nanoscale transport physics, and not nominal material substitution.

2.2. Geometric amplification of barrier/liner volume penalty

The traditional Cu stack relies on barrier and liner layers to provide chemical stability and yet the same layers are geometrically costly at advanced nodes. Even a small fraction of the cross-section can be occupied by a few nanometers of Ta/TaN and liner thickness in a trench that already has a critical dimension of the order of sub-10 nm. Since such layers are far more resistive than Cu, the lost area is not offset by interface conduction; the cumulative line resistance increases far more rapidly than a simple scaling of area would [3]. That is, the geometric price of the barrier stack is nonlinearly proportional to the line size.

The punishment is also increased by interfacial scattering. After the Cu core has been compressed between the barrier/liner stack, a greater portion of carriers will be moving in close proximity to the interfaces, the location of higher diffuse reflection probability. A barrier of the same nominal

thickness will then mean very different things in a 100 nm trench and a 10 nm trench. This is the reason why the key issue of Cu integration is not simply to find a thinner barrier, but rather to find an interface solution that does not ruin the seed process window, the fill process and the end process line resistance simultaneously [3].

2.3. From diffusion blocker to multifunctional interface layer

At more mature nodes, the barrier layer was somewhat equivalent to a unitary-function diffusion blocker: it must be stable, dense, and inert. That definition can never be complete at advanced nodes. A helpful interface layer should at once provide answers to at least four questions: whether it inhibits metal diffusion, whether it allows superior nucleation or direct plating, whether it enhances or degrades electron scattering and contact resistance and whether it enhances or impairs long-term EM, TDDB, and thermomechanical reliability. The barrier/liner stack has become, therefore, a versatile interface-engineering unit.

Materials are evaluated by new criteria with this functional expansion. Certain materials are chemically very good diffusion barriers, but stick poorly to low-k dielectrics; others are electrically desirable and reopen diffusion paths quickly by crystallization or grain-boundary evolution; others do well in straightforward thin-film stacks, but cannot meet realistic CMP, etch, and contamination windows. The key competition in advanced interconnects is no longer how well a particular material can block Cu in a static sense, but how well they can do so with the least geometric cost at the expense of adhesion, transport and reliability. Table 1 summarizes the representative physical parameters of Cu, Co, and Ru and their implications for interface/barrier design.

Table 1. Representative physical parameters of candidate interconnect metals and their interface implications

Metal	Bulk resistivity (μΩ·cm)	Mean free path λ (nm)	Melting point (°C)	Implication for interface/barrier design
Cu	1.68	≈39	1085	Lowest bulk resistivity, but highly sensitive to interface roughness and grain-boundary scattering in narrow lines; must be assessed together with barrier/liner overhead.
Co	≈6.2	≈19	1495	Well suited to local interconnects and single barrier/liner designs, with good EM potential but non-trivial line-resistance and thermal trade-offs.
Ru	≈7.1	≈6.7	2334	Shows a milder size effect at extreme confinement and works naturally with semi-damascene and quasi-barrierless schemes, albeit with tighter process windows.

Note: the values are intended to indicate relative trends in size effect and interface scattering rather than absolute rankings under every process condition; the numbers are primarily based on Ref. [1].

3. Lifetime-extension strategies for barrier and liner layers within the Cu platform

3.1. The coupled limits of Ta/TaN, Cu seed, and electrofill

A strong mix of chemical strength, process maturity and manufacturability is the historical basis of Ta/TaN dominance. TaN prevents the diffusion of the copper and Ta enhances adhesion and offers a superior seed-deposition interface. However, it is precisely this mature stack that is structurally unsuitable for aggressive scaling. Li and others observe that direct electrochemical deposition of Cu over Ta/TaN is impractical due to the high resistivity of the barrier in the sub-20 nm and in particular sub-10 nm trench, and therefore, PVD or CVD seed deposition is essential; when the geometry is in the sub-20 nm and more so sub-10 nm regime, however, non-uniform coverage of the seed is

unavoidable; accordingly, this is not just a weakness of Ta/TaN: it is that the entire downstream fill sequence would be a hostage to a process window that is narrowing all the time.

The traditional stack is also hiddenly expensive in terms of reliability. According to the Co-W study conducted by Oliveira et al., Ta/TaN limits the minimum seed thickness of Cu and that the interfacial energy of Ta/Cu is relatively high and may exacerbate the post-annealing dewetting, which limits the electromigration resistance and thermal stability [4]. This implies that the traditional interface stack not only damages the line resistance, but also morphological stability and defect formation when subjected to further thermal processing. The problem of advanced-node is not simply addressed by merely shearing off a few angstroms of the conventional barrier.

3.2. Conductive alloy barriers: Co-W and Ru-Ta

An obvious extension of the life of the Cu platform is to substitute Ta/TaN with alloys that are more conductive but continue to exhibit significant barrier performance. One example is Co-W. Oliveira et al. demonstrate that Co-W was suggested as a candidate seedless barrier in the case of Cu metallization and may remove a single step of seed-deposition [4]. More to the point, the work emphasizes the fact that the evaluation metric in itself has shifted at advanced nodes: a useful barrier has to not only be able to endure thermal treatment without being catastrophically interdiffused, but also to maintain interfacial morphology and to suppress dewetting to such an extent that the entire plating-and-annealing cycle would be manufacturable.

Ru-Ta represents an analogous yet different strategy wherein Cu wetting and diffusion inhibition is equilibrated by designing alloys. When Torazawa et al. compared RuTa and RuTa(N) they discovered that the incorporation of nitrogen does not necessarily enhance performance; rather RuTa(N) has lower thermal stability, recrystallization and forms a high-angle grain boundary upon annealing, which consequently reduces the performance of barriers and reliability of via-EM [5]. This observation is very educative since it demonstrates that enhanced barrier failure is not necessarily caused by an apparent chemical incompatibility, but rather by thermally-activated microstructural changes that recapitulate rapid diffusion routes in an ultrathin film. The actual difficulty is thus not to synthesize the barrier in a more chemically complex way, but rather to preserve the low-diffusion, low-scattering and high-adhesion state following realistic BEOL thermal histories.

3.3. Atomically thin 2D barriers and graphene-enabled encapsulation

When metallic alloy barriers reach their continuity constraints, two dimensional materials are intrinsically appealing due to their promise of almost zero volume overhead. Lo et al. applied TDDB, STEM-EDS and EELS in their paper on h-BN and MoS2 to show that atomically thin 2D layers are capable of dramatically increasing time-to-breakdown and effectively suppressing diffusion of Cu into the underlying dielectric [6]. What is significant about this finding is that it propelled the notion of a sub-nanometer diffusion barrier to a theory-to-interface engineering bridge. Because traditional TaN barriers are normally limited by a thickness floor of about 2–3 nm, the use of 2D materials is attractive because their geometrical tax is nearly zero.

Simultaneously, the 2D path depicts the interfaces as central as opposed to skipping them. A sheet of 2D can have a large intrinsic diffusion barrier, yet real device failure can be triggered at grain boundaries, transfer defects, damaged edges, or poorly wetted contact points. A complementary view is given by Kuo et al. in their graphene-all-around Co interconnect. They obtained a 27 percent resistance reduction, a 10.8 percent current density boost and a 36-fold improvement in EM lifetime and TDDB measurements validated the diffusion-barrier role of the graphene sheath by making graphene directly around Co within the BEOL thermal budget [7]. This implies that 2D materials in sophisticated interconnects should not be perceived as only replacements to traditional barriers; they can serve as encapsulating interface stabilizers that reconfigures surface diffusion, adhesion and electrical conduction in one. Table 2 compares the representative interface barrier/liner routes in terms of their structural benefits, evidence base, and main limitations.

Table 2. Representative interface barrier/liner routes: structural benefits, evidence base, and main limitations

Route	Core benefit	Main evidence	Current limitation
Ta/TaN + Cu	Mature, reliable, and fully compatible with dual damascene.	Established industrial baseline; Ref. [3] synthesizes seed, fill, and scaling limits.	High resistivity and a non-zero thickness floor create a severe volume penalty; seed non-uniformity ruins fill in ultra-narrow trenches.
Co-W barrier	More conductive than conventional Ta/TaN and potentially directly plateable.	Post-anneal electrical and dewetting analysis of Cu/Co-W stacks in Ref. [4].	Structure-level long-term reliability and process window remain weaker than those of mature Cu flows.
Ru-Ta alloy barrier	Balances Cu wettability with barrier functionality and can relax the fill window.	Comparative barrier-property and EM results for RuTa versus RuTa(N) in Ref. [5].	Nitrogen incorporation can reduce thermal stability and reopen grain-boundary diffusion paths.
2D h-BN / MoS2	Atomic-scale thickness with minimal volume overhead.	TDDB and STEM-EDS/EELS evidence of markedly longer time-to-breakdown in Ref. [6].	Defects, adhesion, wetting, and CMOS compatibility still block large-scale manufacturing.
Co-Ti single barrier/liner	Combines barrier and liner functions, reducing interface count and thickness.	TDDB extrapolation indicates a lifetime increase from 116 days to the order of 32 years [8].	Evidence is concentrated in local Co interconnects and specific dielectric stacks.
Ru-Zn self-forming barrier	Realizes barrier, adhesion, and nucleation benefits through interfacial compounds such as Zn-Si-O.	TDDB, XAS, TEM/EDS, and DFT jointly support the dual-mechanism picture in Ref. [8].	Needs validation in more complex BEOL stacks and porous low-k dielectrics.
Ru semi-damascene	Recovers conductor cross-section by removing the traditional thick barrier/liner stack.	Experimental integration at 18–26 nm pitch and AR 6–8 with thermal-cycle stability [12].	EM, TDDB, and defect statistics are not yet as complete as in mature Cu flows.

4. Paradigm shift in interface engineering during the Cu-to-Co/Ru transition

4.1. Co local interconnects and Co-Ti as a single barrier/liner

Co was originally not designed as a universal metal-level replacement but as a strategic material in contacts and local interconnects with a special emphasis on current density and reliability. Its greater heat of melting and greater cohesiveness among its atoms cause its appeal in the places where a small net rise in nominal resistivity can be exchanged with a higher potential of reliability. The Co0.65Ti0.35 idea presented by Zhou et al. goes one step further and proposes that both barrier and liner functions can be incorporated in a single Co-Ti alloy film, which means that the Ta/TaN or Ti/TiN bilayer can be substituted by a thinner and simpler interface unit [8].

This route is not only important in terms of a reduction of thickness but also the reduction of the number of interfaces. Each extra material interface of a nanoscale interconnect may add a new plane of scattering, a new bonding failure, and a new potential route of rapid diffusion. By means of TDDB analysis, Zhou et al. demonstrated that Co0.65Ti0.35 is able to inhibit a portion of the Co-ion diffusion, slow the formation of conductive-paths and increase the extrapolation of characteristic life to 116 days to the order of 32 years [8]. In practice, the actual value of Co lies not in its being a replacement for Cu; it allows the overall barrier/liner architecture to be simplified and integrated.

4.2. Ru-Zn self-forming barriers and interfacial compound engineering

If Co-Ti represents functional integration, Ru-Zn represents a further step toward reaction-driven interface design. Joi et al. demonstrated that adding Zn into a Ru liner leads to the formation of interfacial compounds such as Zn-Si-O at the dielectric boundary while simultaneously improving adhesion and electrochemical nucleation for Cu [9]. TDDB, XAS, TEM/EDS, and DFT together

support a dual-mechanism picture in which the interface not only blocks transport but also provides a cathodic-protection-like benefit.

It is a significant change in thought. An external blocking layer involves a traditional Ta/TaN layer which is deposited in advance; its value is principally due to geometric separation. An example of a self-forming barrier, Ru-Zn, is based on the reaction product that forms at the desired location. This provides a reduced geometrical penalty and higher tunability. Meanwhile, the larger alloy-screening exercise by Wehring et al. indicates that the problem is already no longer that of identifying low-resistivity materials which prevent the diffusion of Cu. Out of 17 binary and ternary alloys studied, only a very small fraction of them provided acceptable adhesion on both the Cu and SiCOH faces; many otherwise promising barrier materials still needed further liners like Co to fix adhesion [10]. The new bottleneck is thus not only the strength of the barriers but rather the capability to combine low resistivity, strong diffusion inhibition and high dual interface adhesion into a unified interface system.

4.3. Ru interconnects, direct metal etch, and semi-damascene integration

The significance of Ru extends beyond its relatively mild size effect. Ru opens the door to a different patterning paradigm. Already at 48 nm pitch, Zhang et al. reported dual-damascene Ru interconnects with good yield, comparable via resistance behavior, no EM failures, and longer TDDB times, indicating that Ru had early credibility as a post-Cu candidate [11]. At tighter pitches, its most important advantage is that it supports direct metal etch, which is fundamentally difficult for Cu because Cu does not form sufficiently volatile dry-etch products. Decoster et al. explicitly identify Ru and Mo as candidate metals for 32 nm pitch and below in the context of direct metal etch and the corresponding patterning challenges [13].

The strongest current evidence for this architecture shift comes from the semi-damascene module reported by Gupta et al. at IEDM 2023. In a two-metal-level Ru semi-damascene structure with fully self-aligned vias, high-aspect-ratio bottom Ru lines were demonstrated at 18–26 nm metal pitch and CDs of 7–10 nm. At a CD of 10 nm and an aspect ratio of about 6, the line resistance reached approximately 235 Ω/μm, around 75% lower than that of a simulated Cu line that still carried the burden of a 2 nm barrier/liner stack, and the line resistance remained unchanged after 1000 h of thermal cycling between −50 and 125 °C [12]. This is far more than an academic proof of concept: it is evidence that Ru plus a very thin interface layer plus metal-first patterning can form a credible manufacturing route. Yet even here, “barrierless” is not literally barrier-free; an ultrathin adhesion layer remains present, which is why the term quasi-barrierless is more accurate than absolute barrierless.

5. Reliability mechanisms controlled by interface barrier layers

5.1. Electromigration: sealing fast diffusion paths and rearranging transport routes

The root cause of electromigration failure is due to the long-term atomic transport under electron wind forcing, which will eventually lead to the formation of voids around the cathode and the concentration around the anode. Traditionally in Cu interconnects, bulk diffusion paths are not typically the most hazardous, but rather fast paths on the top surface, along the interfaces, and along the grain boundaries. Due to the reduction in size and the increase in ratio of the interface fraction, as the size decreases, the Cu atoms are more susceptible to motion along those routes. The comparison RuTa vs RuTa(N) offers itself as a valuable teaching point: two nominally similar barriers may have vastly different via-EM reliability when annealed to change grain size, grain-boundary nature, and thermal stability [5]. It is not the very presence of a barrier, but the presence of a barrier microstructure that actually blocks the lowest-energy atomic paths, that is the controlling variable.

In Co and Ru systems, the impact of the interface layer is better understood as a re-routing of migration pathways. Co-Ti reduces interface count and improves interface quality [8]; graphene-all-around Co stabilizes surface atoms through C–Co bonding and a continuous sheath, thereby

improving current-carrying capability and EM lifetime [7]. In Ru systems, removing the traditional thick barrier/liner stack and replacing it with a much simpler metal/ultrathin-interface architecture reduces the number of weak fast-diffusion boundaries [11-12]. Thus, the decisive route to longer EM lifetime in advanced interconnects is no longer to search only for a metal with intrinsically better EM resistance, but to design interfaces that no longer provide easy migration shortcuts.

5.2. TDDB: from blocking Cu to suppressing ion sources and defect evolution

In the case of BEOL interconnects, TDDB is not an entirely dielectric problem; rather, it is a metal-dielectric interfacial problem. As soon as Cu-, Co-, or Ru-related ions enter the dielectric, subjected to both electrical and thermal stress, they may modify local trap populations and increase the rate of conductive path formation. Traditional Ta/TaN barriers are useful in the sense that they attempt to physically separate the active metal and the dielectric. But, in the vicinity of their thickness and continuity limits, pure geometry separation is progressively harder to sustain [3]. This is exactly the reason why both Co-Ti and Ru-Zn adopt TDDB as a key measure of reliability.

The Co0.65Ti0.35 data indicate that a single barrier/liner has the capacity to inhibit some of the Co-ion diffusion and considerably hinder the formation of conductive-paths [8]. The Ru-Zn is a step further since interfacial products like Zn-Si-O are formed not only in inhibiting the migration of the metal-ions but also enhances adhesion and electrochemical nucleation, which inhibits the local defect concentration tendency [9]. Mechanistically, the TDDB logic of advanced nodes has thus shifted from depositing a thicker blocking film to making ion sources less probable to form and harder to inject into the dielectric.

5.3. Thermal stability, stress-induced voiding, and adhesion failure

Anything to do with advanced interconnects is never electrical in its reliability. Self-heating, thermal cycling, and thermal-expand mismatch become significant issues on the interfaces as the current density increases and dimensions are reduced. An example of RuTa(N) already demonstrates that a barrier may appear promising in the as-deposited form and become unprofitable due to nitrogen desorption, grain growth, and undesirable grain-boundary evolution [5]. Such a thermally activated microstructural change affects EM, TDDB, and morphology stability in a complex manner. Simultaneously, the barrier-alloy screening work by Wehring et al. demonstrates that most materials with good performance as diffusion blockers do not offer adequate adhesion on the two interfaces, and this fact implies that delamination, cracking, and stress-induced voiding become a reality under thermal cycling [10].

It is specifically appealing that SAM-based interface engineering provides a molecular scale methodology by which thermally driven reactions can be controlled. Although Ru/SAM/Ox/Si stacks were demonstrated to be beneficial in increasing adhesion and significantly slowing interdiffusion of Ru and other undesirable interfacial reactions, direct XPS evidence of SAM retention post-annealing at 700°C was observed [14]. This finding is conceptually significant: a high-end barrier film need not be an inorganic film. Provided that it can survive the pertinent BEOL thermal budget and inhibit undesirable reactions without sacrificing conductivity, it can be used as a legitimate ultrathin barrier-and-adhesion coating. The important question will then not be whether there is an interface layer present or not, but whether the interface will tend towards a more stable or less stable position in realistic thermal histories.

5.4. Reliability metrics and the current evidence boundary

Although Co and Ru routes are encouragingly improving, the current evidence base is still facing a comparability gap. The Ru data at 48 nm pitch [11], the 18 nm-pitch semi-damascene data [12], and the local-structure Co-Ti or graphene/Co results [7-8] all show a particular strength, but are not yet a standard benchmark at the same line width, aspect ratio, dielectric, and stress. The importance of that gap is that the best-case demonstrations alone cannot be used to make technology decisions.

What is now required in the field is not merely more one-off material wins, but appropriately comparable reliability matrices: the same pitch, the same aspect ratio, the same dielectric environment, and the same temperature current stress conditions, and the line resistance, the EM, the TDDB, the delamination and the thermal-cycling statistics are all reported and correlated with interfacial chemistry. It is only then that interface barrier research can be brought beyond a body of compelling case studies to a practical foundation in route choice. Table 3 summarizes the major failure modes of advanced interconnects and the interface-level variables that control them.

Table 3. Major failure modes and the interface-level variables that control them

Failure mode	Main driving force	Interface-related control variables	Representative evidence
Electromigration (EM)	Electron-wind-driven atomic transport and void nucleation.	Fast diffusion paths at top/sidewall interfaces, interface adhesion, and cap/liner continuity.	Reducing interface count or strengthening interfacial bonding in Ru and Co systems can markedly improve lifetime [5], [10-12].
TDDB	Defect accumulation in the dielectric together with metal-ion injection.	Barrier continuity, interfacial chemistry, ion-source formation, and trap evolution in the dielectric.	Direct evidence exists that Co-Ti and Ru-Zn delay the formation of conductive paths [7-8].
Thermal stability	Interdiffusion during annealing, local Joule heating, and BEOL thermal budget.	Reaction barriers, thin-film recrystallization, self-formed interfacial compounds, and SAM retention.	RuTa(N) and SAM routes reveal both the downside and upside of thermally activated interface evolution [5], [14].
SIV/adhesion failure	Thermal-expansion mismatch, self-heating, and mechanical incompatibility across multilayer interfaces.	Adhesion energy, interfacial roughness, low-k compatibility, and minimum adhesion-layer thickness.	The common weakness of many low-resistivity barrier alloys is insufficient adhesion on one or both interfaces [9].

6. Discussion: the triple trade-off among performance, reliability, and manufacturability

6.1. Why low bulk resistivity no longer defines the best interconnect solution

The term best interconnect metal in itself is a misnomer in the context of advanced nodes. Cu has the lowest bulk resistivity, however, its long mean free path, high interfacial scattering sensitivity, and reliance on a comparatively thick barrier/liner stack presently are devastating to its appeal under extreme confinement [1], [3]. Co has superior ability to be used with single barrier/liner ideas and has the potential to be highly reliable in local interconnect conditions, but it cannot be used universally due to its nominal resistivity [8]. Ru has the advantage of a less severe size effect and better compatibility with new patterning schemes, but presents non-trivial issues of direct metal etch, nucleation, wetting, and cost [11-13]. The most desirable line is not determined by the minimum bulk resistivity but by the ideal combination of effective line resistivity, long-term stability, and manufacturability.

This is why the future will likely not be governed by one metal across all levels. Certain highly stressed local layers may favor Co or Co-based alloys, while the tightest-pitch and highest-aspect-ratio levels may be more naturally served by Ru semi-damascene, with wider levels remaining Cu-based for a considerable time. Interface barrier layers are the enablers of that heterogeneous future. Without a credible interface solution, even an otherwise promising metal route cannot become a practical technology option.

6.2. Engineering meaning of barrierless/linerless and the case for “quasi-barrierless”

Barrierless is one of the most widely used and most potentially misleading terms in the recent interconnect literature. In many contexts, it is intended to mean only that the conventional thick Ta/TaN stack has been removed. It does not necessarily mean that the structure contains no functional

interface layer at all. The IEDM 2023 Ru semi-damascene route, for example, still uses an ultrathin TiN adhesion/interface layer even while emphasizing the barrierless/linerless concept [12]. Likewise, Ru-Zn no longer relies on a pre-deposited thick barrier, but it still depends on the formation of interfacial compounds that play a barrier role [9].

There are technological implications of this semantic correction. When it is assumed that the future interconnects will literally be working without any interface layer, the significance of adhesion control, surface-energy engineering, interfacial reaction suppression, and contamination management will be underestimated. When however one understands that the advanced interconnects always need some form of functional interface layer, then the right research question is to determine how to make that layer as thin, conductive, stable, and manufacturable as possible. The second formulation is far more in line with the existing evidence base.

6.3. Research gaps and route judgment for future nodes

Combined, the evidence gives rise to at least three priority directions in the next three to five years. The first priority is to close the reliability data gap for Ru semi-damascene at smaller pitch and higher aspect ratio. The most compelling resistance and thermal-cycling behavior at 18 nm pitch has already been shown to be compelling, but EM, TDDB, SIV, and defect statistics have yet to be reported in a form that would permit a direct comparison with mature Cu baselines [12-13]. The second direction is to move self-forming barriers beyond single-element doping toward programmable interfacial compounds. Ru-Zn has already shown that moving the doping logic from the Cu bulk to the liner/interface level can yield a more controllable combination of adhesion and barrier benefits [9]; the next step is to find multi-component interface chemistries that remain compatible with porous low-k dielectrics while preserving low resistance.

The third direction is the engineering maturation of molecular and 2D interface layers. SAMs and 2D materials provide a compelling vision of nearly zero-thickness interfaces, but their main weakness is no longer isolated proof-of-principle performance. Rather, it is defect tolerance, full-wafer uniformity, compatibility with subsequent etch and CMP steps, and the ability to monitor those interfaces in-line [6], [14-15]. The broader review by Kim et al. offers a useful long-term conclusion: future interconnect competition will not be decided by a single material parameter, but by the co-design of metal, interface layer, and integration architecture [15]. In the case of the topic of this paper, that means that research on interface barriers will not become any less central in the post-Cu age.

7. Conclusion

As discussed in this paper, the development of interface barrier technology in advanced semiconductor interconnects is indicative of a more fundamental change in the philosophy of backend design: the effective line resistance, reliability, and manufacturability of the system as a whole is now the measure of success. The Cu/Ta(TaN) platform crisis is caused by tight sensitivity of Cu to boundary scattering and geometrical and process penalties of stacks of thick barrier/liner. In this connection, Cu-lifetime-extension systems like Co-W, Ru-Ta, atomically thin 2D barriers, and graphene-based encapsulation are useful since they counter that volume penalty and restructure the interface-scattering environment. More to the point, Co-Ti single barrier/liner schemes, Ru-Zn self forming barriers, and Ru semi-damascene designs show that the true future of advanced interconnects is not entirely eliminating interface layers, but redesigning them into thinner, more conductive, more adhesive, and more chemically programmable functional interfaces. In subsequent nodes the interface barriers will not be passive diffusion blockers. They will be the focal points on how much of the electrical performance, long-term reliability and process feasibility can be met concurrently and the path to arrive at that balance with the minimum geometric tax is the one that most likely will characterize the next generation of interconnect technology.

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